[Pulse width control system for transmitting serial data]

Abstract of Disclosure

A pulse width control system includes a serial transmission line for receiving serial data signals and a differential pair having a first transistor and a second transistor. The first and second transistors are connected to the transmission line for respectively producing a positive data signal and a negative data signal. The first and second transistors are respectively controlled by a first control signal and a second control signal, with a differential data signal being produced by subtracting the negative data signal from the positive data signal. First and second delay control cells are connected to the first and second transistors for respectively delaying the first and second control signals. Delay times caused by the first and second delay control cells to delay the first and second control signals are adjusted to ensure that all data pulses of the differential data signal have uniform width.

Figures